A 3.5 WATT HIGH EFFICIENCY FREQUENCY QUADRUPLER FOR X-BAND APPLICATIONS

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ABSTRACT

A microwave integrated circuit X4 frequency multiplier has been developed which has a peak output power of greater than 3.5 watts at 9.5 GHz and a 6 percent 1 dB bandwidth. This performance was achieved with an input power of 12 watts peak at S-band and at 10 percent duty cycle.

Introduction

Two primary goals in the development of solid state transmitter components have been the achievement of high operating efficiencies and small circuit size. This is especially true for components intended for use in airborne equipment such as active element phased array radars. This paper describes the design and performance of a high power, microwave integrated circuit frequency quadrupler with the following design specifications:

P_{IN} = 10.5 watts peak
P_{OUT} = 4.0 watts peak (1.0 watts average)
f_{OUT} = 9.5 GHz (band center)
BW = 9.2 - 9.8 GHz

The quadrupler uses two high power beam-leaded step recovery diodes and was designed in integrated circuit form using alumina microstrip. The final version demonstrated a minimum conversion loss of 5.3 dB with a peak output power of 3.5 watts. The circuit was optimized for use over a 6% bandwidth from 9.2 to 9.8 GHz and demonstrated less than 1.0 dB degradation in efficiency over that band. Finally, the multiplier exhibited only 3 dB variation in efficiency over an input power level variation of approximately 20 dB.

Diode Characteristics

The starting point in multiplier design is the selection of the active device. A silicon step-recovery diode was selected for this application because it offers the highest possible multiplier efficiency when compared with other types of diodes having identical cutoff frequencies. The diode parameters required to satisfy the specifications were determined from relations given by Penfield & Rafuse [1] and Burckhardt [2] and are listed below:

V_{BR} = Diode Breakdown Voltage = 135 volts minimum

C_{jeff} = Effective Junction Capacitance = 0.72 pf

r_s = Diode Small Signal Resistance = 1.2Ω

NOTE: $C_{jeff} = C_{jmin} \frac{1}{1 - (\phi/V_{rp})^{\alpha}}$

The step-recovery diode used in this design is a multiple-chip, series beam-lead diode array intended for high-power multiplier applications. Two arrays in parallel were used to obtain the required diode parameters and to reduce the heat dissipated in each individual device. Since the power level requirements warrant a multiple chip series configuration, the physical form of the device is of critical interest. The basic difficulty in using more than two devices in series is the large parasitic inductances involved in interconnecting them. Also, the fabrication yield of multiple chip circuits can be excessively low. These problems can be solved by using a beam-lead approach to the device design. In this approach, the individual chips are air isolated and are supported in an array by a gold lead frame that also provides electrical connection between the discrete elements. A photograph of the three-section array used in this multiplier is shown in Figure 1. The junction area of each of the three discrete diode chips in the array is of the structure shown in Figure 2. The mesa construction was chosen rather than a planar diffused structure because of the reduction in skin-effect resistance obtained at high frequencies. Such mesa diodes have been used in multipliers up to 30 GHz with very high efficiencies. Because of the beam-lead approach it was necessary to provide a smooth fused-glass bridge to connect the anode beam lead to the mesa contact area. An interdigitated structure was used to subdivide the total junction area and to provide a better distribution of current flow between the anode and cathode contacts.

The one weakness of the beam-lead device is the inherent thermal limitation presented by the beam leads. All the heat from the device must flow through the leads to the heatsink. Although a rigorous analysis of the structure is difficult, predictions indicate that thermal resistances on the order of 50°C/watt are achievable.

All things considered, the low lead inductances and ease of assembly of the beam-lead diode array make it an attractive design approach to a multiplier diode.

Multiplier Circuit Design

Since size was of critical importance in this application, a planar microstrip topology using alumina as a substrate material was selected to minimize circuit area. The basic design of the multiplier was based on previous work reported by Johnson [3], although design differences will be noted. The basic configuration of the multiplier is shown in Figure 3. The circuit design was considered in three steps: input circuit design (f_{in}), output circuit design (f_{out}), and idler circuit design (f_{idl}). Since each step required a knowledge of the large signal parameters of the diode, these parameters were first deduced from Burkhardt's relations [2]:

$$R_{IN} = r_s A \frac{\omega_c}{\omega_o} \quad (1)$$

$$R_L = r_s B \frac{\omega_c}{\omega_o} \quad (2)$$

$$C_{ON} = \frac{C_{MIN}}{S_{ON}/S_{MAX}} \quad (3)$$

$$V_B = V_{ONORM}(V_{RP}) \quad (4)$$

where

R_{IN} = Diode Large Signal Resistance at f_{in}
R_L = Diode Large Signal Resistance at f_{out}
C_{ON} = Diode Large Signal Capacitance at f_N
V_B = Diode Bias Voltage

The parameters are listed in Table I.

TABLE I

LARGE-SIGNAL ELEMENT PARAMETERS OF BEAM-LEAD DIODE ARRAY (TWO IN PARALLEL)

f (GHz)	ωLs (ohms)	$\frac{1}{\omega C_p}$ (ohms)	R (ohms)
2.375	2.8	4.5	25
4.750	5.6	22.5	-
9.500	11.2	11.2	9

The input circuit for this multiplier is a Tchebycheff low-pass matching filter. From published design data [4,5], it was decided that a four element design with a 20 percent bandwidth would be sufficient for this application. Since the circuit design was realized in microstrip, a semi-lumped transmission line network was used to form the inductive and capacitive elements. Referring to Figure 3, the element C_1 is formed by TL1 and TL2, L_1 is formed by TL3, C_2 is formed by TL4 and TL5, and L_2 is formed by a combination of the diode reactance and the reactance of the output circuit at the input frequency. The lengths of transmission line used must be sufficiently short ($<\lambda/8$) to appear lumped at the input frequency.

It can be seen from Table I that the diode impedance at the output frequency (9.5 GHz) is self-resonant. This was an advantage in designing a matching network to match the diode output resistance to the load resistance. Over bandwidths of 10 percent or less, a simple quarter-wave transformer structure is sufficient to provide a 5 to 1 impedance matching ratio with only 0.1 dB rolloff at the band edges. The necessary transformer impedance is given by

$$Z_T = Z_0 Z_L = (9)(50) = 21\,\Omega \quad (5)$$

This transformer is shown as TL6 in Figure 3. It will be noted that a short at the output frequency is provided by TL5 on the input circuit side of the diode. TL5 has a length chosen to be a quarter wavelength at the output frequency for this purpose. This illustrates the necessary multi-function nature of the multiplier circuitry.

The final circuit to be designed was the idler circuit. This circuit was designed to be a closed-loop resonant circuit to allow current to flow through the diode at the idler frequency, and yet not transfer any of the power to a resistive load.

As a final note, the quarter-wave grounded stub shown in Figure 3 (TL7) serves two purposes: it provides a DC bias return path for the diode and it has its impedance selected in such a manner that the sum of the impedances of the output circuit and the diode at the input frequency form the final inductive element of the input matching network. A photo of the final circuit topology is shown in Figure 4. The circuit dimensions are 1.30 inches X 0.55 inches X .025 inches.

Experimental Results

Thirty multipliers were built and tested. Typical performance is detailed below.

Figure 5 shows the detected output power and input VSWR plotted against frequency. These results were taken under the following conditions:

10 Percent Duty Cycle
10 μsecond Pulse Width
12 Watts Peak Input Power
2.3 to 2.45 GHz Input Frequency
Optimum DC Fixed Bias Voltage

NOTE: In this specimen +54V; typically 51 to 57V

Best measured conversion loss (C_L) was 5.3 dB (after subtracting connector losses) at an output frequency of 9.4 GHz. Maximum loss was 6.3 dB at 9.2 GHz. This degradation in C_L over the frequency band is typical of the multipliers tested. Typical units were flat to within 0.8 dB while the worst ones showed 1.5 dB degradation. To achieve this flatness across the whole band, approximately 0.4 dB of C_L was sacrificed. The multiplier could be tuned to have a 4.9 dB C_L at one frequency point with a 3 dB degradation at the band edges.

Conversion loss was measured with the same basic conditions as outlined above for input powers between 125 mw peak and 12 watts peak. The results showed that the units would operate without significant change in bandwidth over the above input power range. (Diode bias voltage was set for each input power level). With 250 mw peak input power, the minimum measured C_L was 6.0 dB; with 125 mw peak input power, the minimum C_L increased to 8.5 dB. C_L was relatively constant over the input power range 500 mw peak to 12 watts peak.

The effect of duty cycle on conversion loss was measured on two multipliers at a pulse width of 200μ-seconds at 10 watts peak input power. Results are included in Table II.

TABLE II
EFFECT OF DUTY CYCLE ON CONVERSION LOSS

Pulse Width (us)	Duty Cycle (percent)	Conversion Loss	
		Unit #1	Unit #2
200	10	5.3 dB	5.4 dB
200	20	5.6 dB	5.7 dB
200	25	--	6.0 dB
200	40	6.7 dB	7.4 dB

Conclusions

A high power, high efficiency X-band quadrupler using alumina microstrip circuitry has been designed and tested. The frequency multiplier uses an air isolated beam-lead step recovery diode array specifically designed for high power applications. The final circuit demonstrated 5.3 dB minimum conversion loss over a 6% bandwidth with 3.5 watts maximum peak power output. The dynamic range of the multiplier was approximately 20 dB (125 mw to 12 watts peak input power range).

Acknowledgments

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REFERENCES

1. Penfield, P. and R.P. Rafuse, Varactor Applications, MIT Press, 1962.

2. Burckhardt, C.B., "Analysis of Varactor Frequency Multipliers for Arbitrary Capacitance Variation and Drive Levels," BSTJ, April, 1965, pp. 675-692.

3. Johnson, Kenneth M., "A High-Performance Integrated Microwave Circuit Frequency Quadrupler," IEEE Trans. on Microwave Theory and Tech., Vol. MTT-16, No. 7, July, 1968, pp. 420-424.

4. Matthaei, G.L., "Tables of Chebyshev Impedance Transforming Networks of Low Pass Filter Form," Proc. of IEEE, Aug., 1964, pp. 939-963.

5. Matthaei, G.L., L. Young, and E.M.T. Jones, Microwave Filters, Impedance Matching Networks and Coupling Structures, McGraw Hill, Inc., New York, 1964.

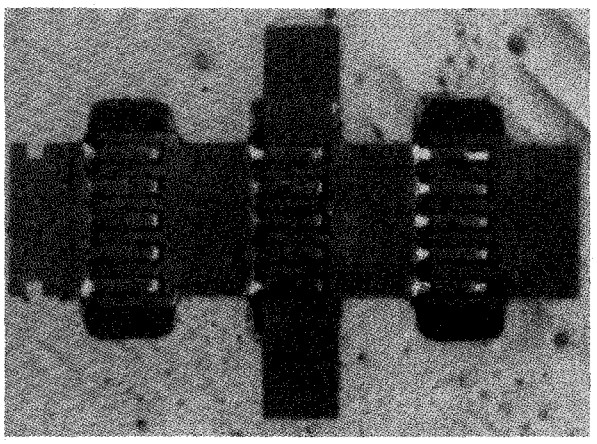


Figure 1. Beam-Lead Step Recovery Diode Array

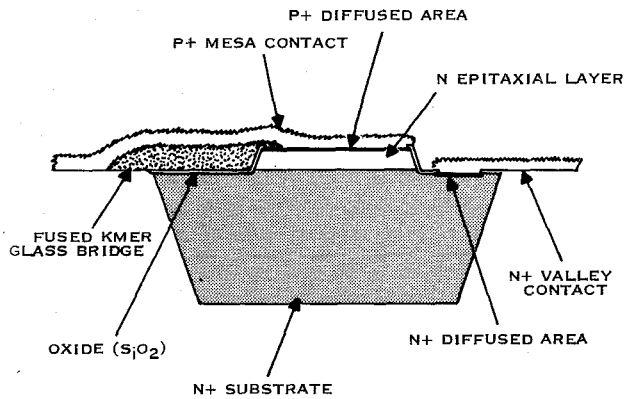


Figure 2. Mesa Diode Array Chip Lateral Cross Section (One Chip)

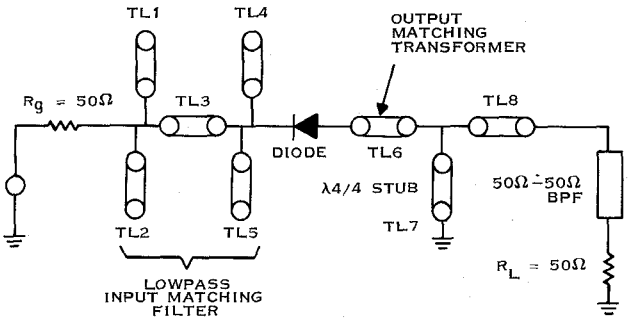


Figure 3. Series Multiplier Schematic

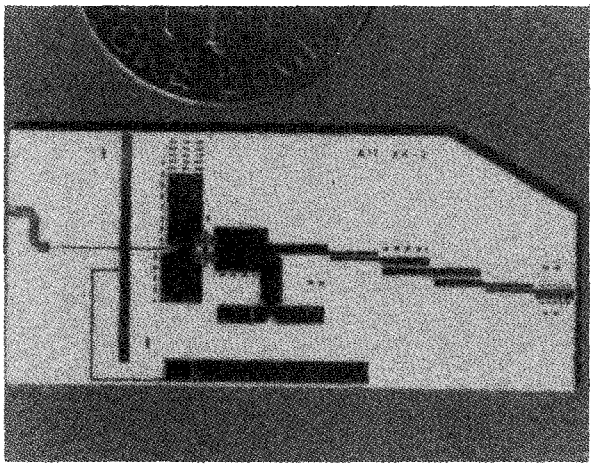
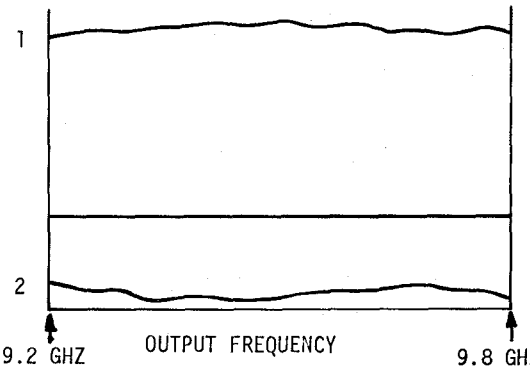


Figure 4. MIC Quadrupler Circuit



1 UPPER TRACE: OUTPUT POWER VERSUS FREQUENCY

2 LOWER TRACE: VSWR VERSUS FREQUENCY

FREQUENCY GHZ	CONVERSION LOSS DB	PEAK OUTPUT POWER WATTS
9.4	5.3	3.54
9.2	6.3	2.81
9.8	5.9	3.1
INPUT VSWR, LESS THAN 1.3:1.		

Figure 5. Multiplier Output Power and VSWR vs. Frequency